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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
DILLON, SAMUEL A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,645	LIOU, MING-SHI	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/10/04* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/707,645 has a total of 18 claims pending in the application; there are 3 independent claims and 15 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

3. As required by M.P.E.P. ' 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed in February 27, 2003.

III. INFORMATION CONCERNING DRAWINGS

4. The drawings are objected to because Figure 7A and Figure 7b list the size of Memory module 80D as 521MB, while every other memory module is a power of 2 (e.g. 32MB, 64MB, 128MB, 256MB). The Examiner surmises that the intended size is 512MB. This objection can be withdrawn with further clarification or correction.

5. The drawings are additionally objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claim 18 discloses a plurality of XOR gates, which are not found in the drawings *(such as Figure 6, which shows a plurality of NXOR gates)*. Therefore, the XOR gates

disclosed in Claim 18 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

6. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

IV. OBJECTIONS TO THE APPLICATION

Abstract / Specification

7. The disclosure is objected to because it contains numerous typographic, spacing and other small errors. The following examples are listed but are by no means intended to provide a comprehensive list of errors:

a. The abstract reads "bbuilding asingle" on line 7, and should be corrected to read "building a single".

b. The specification reads "wwhole" on line 3 of paragraph 7, and should be corrected to read "whole".

c. The specification reads "iincreased incrementallyfrom" on line 6 of paragraph 7, and should be corrected to read "increased incrementally from".

Appropriate correction is required. Applicant's cooperation is requested in correcting any further errors of which applicant may become aware of in a rereading of the specification.

8. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

d. **Claim 8** recites the limitation *"... and if **after** sorting, the size of a first section is equal to the size of a second section, the first and the second sections capable of being swapped."* The Examiner interprets this limitation as claiming that once the sorting is completed, two sections with equal size may be swapped independently of the sorted action.

The Examiner notes that the specification discloses *(page 40 line 18 to page 42 line 9)* that there exist different outcomes to the sorting algorithm that will order the sections in different ways, including swapping of two equally sized sections. The Examiner does not find disclosure relating to the memories being swapped after the sorting operation, and

subsequently does not find the necessary written description for the phrasing *"... and if after sorting ... the first and second sections capable of being swapped"*.

The Examiner notes that this objection may be withdrawn by adding proper antecedent basis for the claimed subject matter in the specification, or amending Claim 8 to read *"sorting the sections by size so as to make the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size, and if* ***during*** *sorting, the size of a first section is equal to the size of a second section, the first and the second sections capable of being swapped."*

e. **Claim 18** recites the limitation "a plurality of XOR gates", which is not disclosed in the specification. The Examiner notes that the specification discloses using NXOR gates where the claim uses XOR gates *(paragraph 35)*, and the objection would be withdrawn if the claimed uses of "XOR" were amended to read "NXOR". For the purposes of further examination, the claims will be read as such.

Claims

9. **Claims 1, 8, 12 and 17** are objected to because of the following informalities:

a. Claim 1 reads "bbuilding asingle" on line 10 of the claim, and should be amended to read "building a single".

b. Claim 8 reads "Amemory" on line 1 of the claim, and should be amended to read "A memory".

c. Claim 8 reads "ssorting, thesize" on line 10 of the claim, and should be amended to read "sorting, the size".

d. Claim 12 reads "sso thatthe" on line 3 of the claim, and should be amended to read "so that the".

e. Claim 17 reads "ssection inthe" on line 2 of the claim, and should be amended to read "section in the".

Appropriate correction is required.

V. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC ' 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 1, 8 and 18** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. Lines 12-15 of **Claim 1** and 15-18 of **Claim 8** discloses *"comparing* ***if at least one comparative bit of the given address matches those in*** *any of the bit-patterns so as to determine the given address is located in one of the sections*

based on the comparison". The Examiner interprets this limitation to be claiming that if at least one comparative bit of the given address matches those in any of the bit-patterns, then it is determined the given address is located in the associated section.

The Examiner notes that Figure 5 and associated discussion in paragraph 34 of the specification disclose that to determine that an address is in a section each comparative bit of the address will need to match the bit-mask. Paragraph 34 discloses that comparison unit 112C will output a result of "true" to reflect the fact that the given address is located in the memory module 80D, but if the claimed test *"if at least one comparative bit of the given address matches those in any of the bit-patterns"* is used then each of the comparison units will output a result of "true", in that bit 31 ('0') of the address matches bit 31 of each of the bit-patterns.

This rejection may be withdrawn pending further clarification or amending Claim 1 and Claim 8 limitations to read "*comparing* ***the given address against*** *any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison".*

5. **Claim 18** discloses a plurality of **XOR** gates receiving a masked address and a standard address generated from the bit patterns. XOR gates inherently will output a logical 1 if the two inputs are not the same (e.g. one is logical 0 and the other is logical 1), so in this case each XOR gate will output a logical 1 if and only if the input address bits are logical opposites. Claim 18 then discloses a second level AND gate aggregating the response of all of the plurality of the XOR

gates. The AND gate will check to see if every output of the XOR gates is 1, which will be the case when each bit pair of the masked address and the corresponding address are different.

Accordingly, the comparison module described in Claim 18 will output a logical 1 if and only the masked address is the logical opposite of the corresponding address. The Examiner asserts that one with ordinary skill in the art would fail to understand how the claimed component would enable determining whether a given address is located in one of a plurality of sections.

Claim Rejections – 35 USC ' 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. **Claims 1-13** are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

8. As per **Claims 1 and 8**, the claimed inventions are directed towards an abstract idea, per se, but do not transform an article or physical object to a different state or thing and do not produce a tangible result. To direct the claimed inventions to statutory subject matter, the claims must be amended to include performing a physical transformation that produces a tangible result, such as storing the corresponding address, the single bit-pattern or the result of the determination in a memory.

9. As per **Claims 2-7 and 9-13**, the additional limitations disclosed do not direct the claimed inventions towards statutory subject matter. To direct the claimed inventions to statutory subject matter, the Examiner directs the applicant to the 35 U.S.C. 101 rejection of Claims 1 and 8 above.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 103 – Koos, Schmisseur, Hirschberg

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 1-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Koos *(US Patent Number 4,400,794)* in view of Schmisseur et al. *(US Patent Number 6,128,718)* and Hirschberg *("Data Compression")*.

12. As per **Claim 1**, Koos discloses

a memory address decoding method for determining if a given address *(memory address location, column 1 line 22)* is located in one of a plurality of sections *(memory boards, column 1 line 13)*, each section having a plurality of memory units and each memory unit having a unique corresponding address *(memory locations, column 1 line 18)*, the corresponding address using the binary system *(column 1 lines 39-44)*,

the method comprising: determining if the given address is located in one of the sections *(column 3 lines 20-62)*.

Koos does not disclose building a single bit-pattern for each section from all corresponding addresses; and comparing if at least one comparative bit of the given address matches those in any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison.

Schmisseur discloses

building a single bit-pattern *("a single bit-pattern" is interpreted to be claiming exactly one bit-pattern, as opposed to a pattern consisting of a single bit)* for each section from all corresponding addresses *(column 4 lines 55-59)*; and

if the comparative bits *(additional addressing bits, column 4 line 65)* of the given address matches those in a bit-pattern, the given address is located in the section based on the comparison *(column 4 lines 55-59)*.

Koos and Schmisseur are analogous art in that they both deal with memory mapping and addressing. At the time of the invention it would have been obvious to use Schmisseur's base address register as the means Koos uses to describe a memory's size and start address.

The motivation for doing so would have been that Schmisseur's register provides a proper response to address space queries by host processors that use procedures such as the one defined by the PCI Specification *(Schmisseur, column 8 lines 40-43)*.

Therefore it would have been obvious to combine the system of Koos with Schmisseur's base address register for the benefit of responding correctly to PCI conforming devices.

Koos and Schmisseur disclose using a prefix address register to keep track of the common address shared by all the memory locations inside a specific memory board *(Schmisseur, column 5 lines 35-60)*.

Koos and Schmisseur do not disclose making the corresponding address in a section with greater size smaller than the corresponding address in a section with smaller size *(this limitation is interpreted as not requiring that there be a section with a greater size than another section, but rather that if there does exist a section with greater size than another section, then the section with a greater size has it's corresponding address be made smaller than the section it is greater than)*. Schmisseur additionally does not disclose how the prefix addresses are assigned.

Hirschberg discloses assigning prefix codes to a collection of weighted elements by sorting them in decreasing weighted order *(Hirschberg, section 3.1)*.

Accordingly, Hirschberg discloses

> making the corresponding address in a section with greater size smaller than the corresponding address in a section with smaller size *(Hirschberg, section 3.1 lines 1-2)*.

Koos, Schmisseur and Hirschberg are analogous art in that Koos and Schmisseur assign prefix addresses to a plurality of differently sized memories,

and Hirschberg teaches an optimal way of assigning prefix codes to a plurality of weighted elements *(Hirschberg, "Shannon-Fano Coding", section 3.1)*.

At the time of the invention it would have been obvious to one with ordinary skill in the art to modify the memory mapping system taught by Koos and Schmisseur to assign the prefix codes using the Shannon-Fano algorithm, as taught by Hirschberg.

The motivation for doing so would have been that Koos discloses wanting to use the least number of significant bits during calculation *(Koos, column 2 lines 64-66)*, and assigning the prefix codes using the Shannon-Fano algorithm technique yields minimal prefix codes for each element *(Hirschberg, section 3.1, lines 6-7)*.

Therefore, it would have been obvious to assign the prefixes of Koos and Schmisseur using the Shannon-Fano algorithm as taught by Hirschberg for the benefit of yielding minimal prefix codes, to obtain the invention of Claim 1.

13. As per **Claim 2**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 1 wherein

> the sections are a plurality of memory modules *(interpreted as that the plurality of sections are a plurality of memory modules as opposed to each section being a plurality of memory modules, Koos, memory boards, column 1 lines 36-38)*.

14. As per **Claim 3**, Koos, Schmisseur and Hirschberg disclose The memory address decoding method of Claim 1 wherein

the single bit-pattern is built for each section, the bit-pattern consisting of all common bits of the corresponding addresses in each section *(Schmisseur, column 4 lines 55-59)*.

15. As per **Claim 4**, Koos, Schmisseur and Hirschberg disclose The memory address decoding method of Claim 1 wherein

if the comparative bits of the given address do not match the bit-pattern bit in any section, the given address is not located in the section, otherwise the given address is located in the section *(inherent in Schmisseur, column 4 lines 55-59)*.

16. As per **Claim 5**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 1 wherein

the sections of same size can be swappable *(Hirschberg discloses the elements being listed in order of non-increasing probability, which inherently does not render incapable the possibility of elements with the same probability being in any order, section 3.1, lines 1-2)*.

17. As per **Claim 6**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 1 wherein

the corresponding addresses in each section increase or decrease in sequence so that the difference between one corresponding address and its previous corresponding address will be a fixed value *(Koos discloses the continuous memory address range being made up of an array of bytes, whose lengths are inherently fixed, column 3 lines 20-24)*.

18. As per **Claim 7**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 1 wherein

the size of each section is a power of 2 *(Koos, column 1 line 32)*.

19. As per **Claim 8** Koos, Schmisseur and Hirschberg disclose a memory address decoding method for

determining whether a given address *(Koos, memory address location, column 1 line 22)* is located in one of a plurality of sections *(Koos, memory boards, column 1 line 13)*, each section having a plurality of memory units and each memory unit having a unique corresponding address *(Koos, memory locations, column 1 line 18)*, the corresponding address using the binary system *(Koos, column 1 lines 39-44)*, the method comprising:

sorting the sections by size so as to make the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size *(Hirschberg, section 3.1 lines 1-2)*, and if after sorting, the size of a first section is equal to the size of a second section, the first and the second sections capable of being swapped *(Hirschberg discloses the elements being listed in order of non-increasing probability, which inherently does not render incapable the possibility of elements with the same probability being in any order, section 3.1, lines 1-2)*;

building a single bit-pattern for each section from all corresponding addresses *(column 4 lines 55-59)*; and comparing if at least one

comparative bit *(additional addressing bits, column 4 line 65)* of the given address matches those in any of the bit-patterns so as to determine in which one of the sections the given address is located based on the comparison *(column 4 lines 55-59)*.

20. As per **Claim 9**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 8, wherein

the sections are a plurality of memory modules *(interpreted as per the rejection of Claim 2, Koos, memory boards, column 1 lines 36-38)*.

21. As per **Claim 10**, Koos, Schmisseur and Hirschberg disclose The memory address decoding method of Claim 8 wherein

the single bit-pattern is built for each section, the bit-pattern consisting of all common bits of the corresponding addresses in each section *(Schmisseur, column 4 lines 55-59)*.

22. As per **Claim 11**, Koos, Schmisseur and Hirschberg disclose The memory address decoding method of Claim 8 wherein

if the comparative bits of the given address do not match the bit-pattern bit in any section, the given address is not located in the section, otherwise the given address is located in the section *(inherent in Schmisseur, column 4 lines 55-59)*.

23. As per **Claim 12**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 8 wherein

the corresponding addresses in each section increase or decrease in sequence so that the difference between one corresponding address

and its previous corresponding address will be a fixed value *(Koos discloses the continuous memory address range being made up of an array of bytes, whose lengths are inherently fixed, column 3 lines 20-24)*.

24. As per **Claim 13**, Koos, Schmisseur and Hirschberg disclose the memory address decoding method of Claim 8 wherein

the size of each section is a power of 2 *(Koos, column 1 line 32)*.

25. As per **Claim 14**, Koos, Schmisseur and Hirschberg disclose a control circuit of memory address decoding for

determining whether a given address *(Koos, memory address location, column 1 line 22)* is located in one of a plurality of sections *(Koos, memory boards, column 1 line 13)*, each section having a plurality of memory units and each memory unit having a unique corresponding address *(Koos, memory locations, column 1 line 18)*, the corresponding address using the binary system *(Koos, column 1 lines 39-44)*, the control circuit comprising:

an access module *(Koos, address bus 14, Figure 1)* for receiving the given address;

making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size *(Hirschberg, section 3.1 lines 1-2)*, and if the size of a first section is equal to the size of a second section, the first and the second sections are capable of being swapped *(Hirschberg discloses the elements being listed in order of non-increasing probability, which inherently does not render*

incapable the possibility of elements with the same probability being in any order, section 3.1, lines 1-2); and

a comparing module *(Koos, Figure 2)* for building a bit-pattern for each section based on its corresponding addresses *(Schmisseur, column 4 lines 55-59)* and sending a plurality of comparison signals after comparing the given address with those of each bit-pattern *(Koos, Figure 3)*.

Koos, Schmisseur and Hirschberg disclose using an algorithm *(Hirschberg, "Shannon-Fano coding", section 3.1)* for making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size, but do not disclose using a sorting module to do the same.

Koos, Schmisseur, Hirschberg and the concept of implementing algorithms as modules are analogous art in that Koos discloses using a module for comparing *(Koos, Figure 3)*. At the time of the invention it would have been obvious to one with ordinary skill in the art to implement the Shannon-Fano algorithm as taught by Hirschberg as a hardware sorting module.

The motivation would have been that the rest of Koos's system was implemented in hardware. Accordingly, implementing the Shannon-Fano algorithm in hardware would have not significantly modified the system architecture.

Therefore, it would have been obvious to implement the sorting algorithm taught by Koos, Schmisseur and Hirschberg as a hardware sorting module for

the benefit of minimal modification to the system, to obtain the invention of Claim 14.

26. As per **Claim 15**, Koos, Schmisseur and Hirschberg disclose the control circuit of Claim 14 further comprising

a logic module *(Koos, element 30, Figure 2)* responsible for receiving the comparison signals and sending a decoding result to determine the given address is located in one of the sections *(Koos, board enable command 32, Figure 2)*.

27. As per **Claim 16**, Koos, Schmisseur and Hirschberg disclose the control circuit of Claim 14, wherein

the sections are a plurality of memory modules *(interpreted as per Claim 2, Koos, memory boards, column 1 lines 36-38)*.

28. As per **Claim 17**, Koos, Schmisseur and Hirschberg disclose the control circuit of Claim 14 wherein

the single bit-pattern is built for each section, the bit-pattern consisting of all common bits of the corresponding addresses in each section *(Schmisseur, column 4 lines 55-59)*.

Claim Rejections - 35 USC ' 103 – Koos, Schmisseur, Hirschberg, Matz

29. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Koos *(US Patent Number 4,400,794)*, Schmisseur et al. *(US Patent Number 6,128,718)* and Hirschberg *("Data Compression")* as applied to Claim 14 above, and in further view of Matz *("Binary Operations")*.

30. As per **Claim 18**, Koos, Schmisseur and Hirschberg disclose the control circuit of Claim 14 wherein the comparing module comprises a plurality of comparing units *(Koos, Figure 1)*, each comparing unit comprising a plurality of first level AND gates *(Koos, NAND gates are AND gates before the inversion, Figure 2, elements 28)*, each of the first level AND gates having two inputs for respectively receiving a mask bit generated from the bit-patterns *(Koos, Figure 2, lines from element 26)* and an associated bit of the given address *(Koos, Figure 2, lines from element 24)*,

They additionally disclose if the comparative bits of the given address matches those in a bit-pattern, the given address is located in the section based on the comparison *(see the 35 U.S.C. 103 rejection of Claim 1 above)*.

Koos, Schmisseur and Hirschberg do not disclose a plurality of XOR gates, and a second level AND gate, each of the XOR gates having two inputs for respectively receiving the output of one of the first level AND gates and a standard address generated from the bit-patterns, the inputs of the second level AND gate being connected to the outputs of the XOR gates and thereby sending out the comparison signals.

Handy discloses a plurality of XOR gates *(Handy, gates below the word Address, upper right corner, Figure 1.10)*, and a second level AND gate *(Handy, gate outputting to the words Match Output, Figure 1.10)*, each of the XOR gates having two inputs for respectively receiving the output of one of the first level AND gates *(Handy, lines from M Tag Bits, Figure 1.10)* and a standard address generated from the bit-patterns *(Handy, lines from M Data Outputs, Figure 1.10)*,

the inputs of the second level AND gate being connected to the outputs of the XOR gates and thereby sending out the comparison signals *(Handy, signal "Match Output", Figure 1.10)*.

Koos, Schmisseur, Hirschberg and Handy are analogous art in that they deal with comparing the upper portion of an address against a generated pattern. At the time of the invention it would have been obvious to use Handy's comparator design to implement the bit mask comparison of Koos, Schmisseur and Hirschberg.

The motivation for doing so would have been that Handy's implementation is a simple comparator consisting of very few gates *(Handy, Figure 1.10 and description)*.

Therefore, it would have been obvious to implement the comparison described in Koos, Schmisseur and Hirschberg using Handy's comparator for the benefit of using a simple design with few gates, to obtain the invention of Claim 18.

VII. REJECTIONS BASED ON DOUBLE PATENTING

31. The following forms the basis for all non-statutory double patenting rejections set forth in this Office action:

> The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In*

re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

32. **Claims 1-4, 8-11 and 14-17** are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over Claims 1-2, 4-5, 12-14 and 16 of copending Application No. 10/708103 in view of Hirschberg *("Data Compression")*. This is a **provisional** obviousness-type double patenting rejection.

33. The Examiner notes that though the inventive entities are different, the assignee for both applications is Via Technologies Inc.

34. Claim 1 is compared to Claim 1 of the copending Application in the following table:

Instant Application	Copending Application
A memory address decoding method for determining if a given address is located in one of a plurality of sections, each section having a plurality of memory units and each memory unit having a unique corresponding address, the corresponding address	A memory address decoding method for determining if a given address is located in one of a plurality of sections, each section having a plurality of memory units and each memory unit having a unique corresponding address, the corresponding addresses

using the binary system, the method comprising:	using the binary system, the method comprising:
building a single bit-pattern for each section from all corresponding addresses; and	building at least one bit-pattern for each section from the corresponding addresses respectively; and
comparing if at least one comparative bit of the given address matches those in any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison.	comparing if at least one comparative bit of the given address matches any of the bit-patterns so as to determine that the given address is located in one of the sections based on the comparison.

35. The copending Application discloses building a pit-pattern for each section from the corresponding addresses, which is a pattern distilled from all the addresses corresponding to that section. This is interpreted as claiming building a pattern that represents all of the common bits that are shared by each address in a section.

The copending Application does not disclose making the corresponding address in a section with greater size smaller than the corresponding address in a section with smaller size.

Hirschberg discloses making the corresponding address in a section with greater size smaller than the corresponding address in a section with smaller size *(section 3.1 lines 1-2)*.

The copending Application and Hirschberg are analogous art in that they both deal with binary prefix codes. At the time of the invention it would have been obvious to assign the copending Application's bit-patterns using Hirschberg's algorithm.

The motivation for doing so would have been that Hirschberg's algorithm yields minimal prefix codes *(section 3.1 lines 6-7)*.

Therefore, it would have been obvious to combine the copending Application's memory address decoding method with Hirschberg's prefix assignment algorithm for the benefit of yielding minimal bit-patterns, to obtain the invention of Claim 1.

36. The following table lists further claims that are provisionally rejected and their counterparts in the copending Application.

Instant Application	**Copending Application**
Claim 2	Claim 2
Claim 3	Claim 4
Claim 4	Claim 5
Claim 8	Claim 1 in view of Hirschberg
Claim 9	Claim 2
Claim 10	Claim 4

Claim 11	Claim 5
Claim 14	Claim 12 in view of Hirschberg
Claim 15	Claim 13
Claim 16	Claim 14
Claim 17	Claim 16

IX. RELEVANT ART CITED BY THE EXAMINER

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chambers *(US Patent Number 7,013,355)* discloses an incremental or bit by bit address decode scheme.

Sherman *(US Patent Number 6,389,507)* discloses a content addressable memory using a search tree to reduce the total number of entries that must be matched against the key.

Steiner *(US Patent Number 3,938,100)* discloses an apparatus for forming an absolute address for accessing the memory of a computer.

Rodman *(US Patent Number 4,587,610)* discloses an address translation method that stores data in association with a tag defining its location in a main memory.

Mitchell et al. *(US Patent Number 4,965,720)* disclose a prefix register associated with each of the address registers to hold a high-order address portion.

Sykora *(US Patent Number 4,860,252)* discloses a self-adaptive computer memory address allocation apparatus.

Aakre et al. *(US Patent Number 4,730,251)* disclose an automatic address assignment system.

Finnell et al. *(US Patent Number 4,654,787)* disclose automatically locating RAMs of various sizes in a memory space.

Schwartz *(US Patent Number 4,468,729)* discloses an automatic memory module sensing and address assignment system.

Thorsrud *(US Patent Number 4,234,934)* discloses an apparatus for scaling addresses received by a memory module.

Kaufman *(US Patent Number 4,025,903)* discloses calculating memory address boundaries automatically.

Bernstein et al. *(US Patent Number 3,982,231)* disclose prefixed storage areas assigned to predetermined blocks of storage.

Steiner et al. *(US Patent Number 3,938,100)* disclose a virtual addressing apparatus for addressing the memory of a computer utilizing associative addressing techniques.

Huffman *("A Method for the Construction of Minimum-Redundancy Codes")* discloses a method for constructing minimum-redundancy codes.

X. CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

38. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). CLAIMS REJECTED IN THE APPLICATION

39. Per the instant office action, Claims 1-18 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571-272-8010. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sam Dillon
Examiner
Art Unit 2185

SAD

DONALD SPARKS
SUPERVISORY PATENT EXAMINER